



(12)

## EUROPEAN PATENT APPLICATION

(43) Date of publication:  
31.05.2000 Bulletin 2000/22

(51) Int Cl. 7: H01L 23/495

(21) Application number: 99309372.3

(22) Date of filing: 24.11.1999

(84) Designated Contracting States:  
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU  
MC NL PT SE  
Designated Extension States:  
AL LT LV MK RO SI

(30) Priority: 26.11.1998 JP 33509898

(71) Applicant: SHINKO ELECTRIC INDUSTRIES CO.  
LTD.  
Nagano-shi, Nagano 380-0921 (JP)

(72) Inventors:  
• Muramatsu, Shigetsugu,  
Shinko Elect. Ind. Co. Ltd.  
Nagano-shi, Nagano 380-0921 (JP)  
• Ogawa, Yoshihiko, Shinko Elect. Ind. Co. Ltd.  
Nagano-shi, Nagano 380-0921 (JP)  
• Kojima, Norio  
Yokohama-shi, Kanagawa 235-0045 (JP)

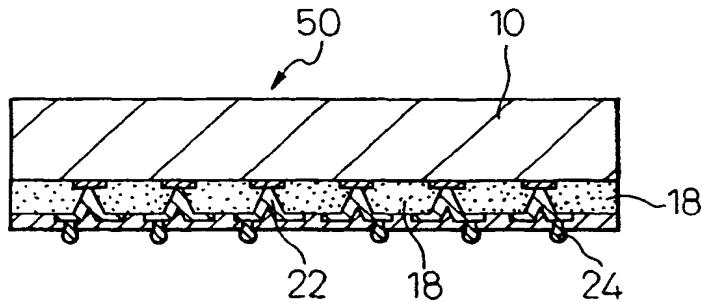
(74) Representative: Rackham, Stephen Neil  
GILL JENNINGS & EVERY,  
Broadgate House,  
7 Eldon Street  
London EC2M 7LH (GB)

### (54) Metal foil having bumps, circuit substrate having the metal foil, and semiconductor device having the circuit substrate

(57) A semiconductor device wherein a circuit substrate of a single or multiple layer is composed in such a manner that bumps (22), which are electrically connected to connection electrodes (12) provided on one face of a surface mount device (10), are arranged in the same planar arrangement as that of the connection electrodes (12). The bumps (22) protrude from one side

of a sheet of metal foil (20) on which wiring patterns (16) electrically connected to the bumps (22) are formed. An insulating adhesive agent layer (18) is adhered to the side of the sheet of metal foil (20) having the bumps (22) and is also adhered to one face of the surface mount device (10) while the tips of the bumps (22) come into contact with respective connection electrodes (12).

Fig.19(c)



**Description**

**[0001]** The present invention relates to a sheet of metal foil having bumps, a circuit substrate having the sheet of metal foil, and a semiconductor device having the circuit substrate which are used for manufacturing a semiconductor chip.

**[0002]** A chip size package is a semiconductor device, the size of which is substantially the same as that of a semiconductor chip. Therefore, the chip size package is characterized in that the mount area can be remarkably reduced. In this chip size package, it is necessary to provide an arrangement by which thermal stress generated between the mount substrate and the semiconductor chip is reduced. Accordingly, various arrangements to reduce the thermal stress have been proposed.

**[0003]** Electrode terminals of the semiconductor chip are very fine and arranged very densely. On the other hand, external connection terminals such as solder balls are larger than the electrode terminals. Therefore, it is necessary to arrange the external connection terminals in such a manner that the arranging intervals of the external connection terminals are longer than those of the electrode terminals, and the external connection terminals are usually arranged on the overall electrode terminal carrying surface in the formation of an area array.

**[0004]** Fig. 22 is a view showing an example of the arrangement of the electrode terminals 12 of the semiconductor chips 10 and also showing an example of the arrangement of the lands 14 to which the external connection terminals such as solder balls are joined. The lands 14 are arranged in such a manner that the arranging intervals of the lands 14 are longer than those of the electrode terminals 12, and the electrode terminals 12 and the lands 14 are electrically connected with each other by the wiring sections 16.

**[0005]** When the land 14 is connected to the external connection terminal, it is common to adopt an arrangement having a cushioning function which is composed in such a manner that, for example, a metal post is vertically attached onto the land 14 and the external connection terminal is joined to an upper end portion of the metal post. Also, the following arrangement is adopted. On an electrode terminal carrying surface of the semiconductor chip, there is provided a buffer layer for reducing thermal stress, and a land of the wiring pattern film, which has been made to adhere via the buffer layer, is joined to the external connection terminal such as a solder ball, so that the cushioning function can be provided.

**[0006]** In the case of a circuit substrate on which a flip chip type of semiconductor chip is mounted, or in the case of a mount substrate on which a surface mount device such as a chip size package is mounted, the connection electrodes such as solder bumps are very densely arranged. Therefore, it is impossible to electrically connect all the connection electrodes to the wiring

patterns when the wiring layer is formed into a single layer. For the above reasons, the wiring patterns are formed into a multiple layers in the above cases.

**[0007]** In order to form the circuit substrate into a multiple layers, there is provided a buildup method in which wiring patterns, which are interposed between insulating layers, are electrically connected with each other while the insulating layers are being successively laminated so that a multiple layer can be formed. Also, there is provided a method in which a multilayer of circuit substrates, on which the vias and the wiring pattern are previously formed, are laminated on each other so that a multiple layer can be formed.

**[0008]** In this connection, in order to manufacture a semiconductor device having a fine pattern such as a chip size package, it is necessary to conduct machining with high accuracy.

**[0009]** For example, in the case where wiring is conducted on the electrode terminal carrying surface of the semiconductor chip so as to form the connection electrode having a predetermined pattern and an external connection terminal is joined to the connection electrode, it is necessary to conduct fine machining in which metal posts for supporting the external connection terminals are formed. In the case where an insulating layer having a wiring pattern, which is also used as a buffer layer, is formed on the electrode terminal carrying surface of the semiconductor chip, it is necessary to provide a wire bonding process or a lead bonding process for electrically connecting the electrode terminals of the semiconductor chip with the wiring patterns.

**[0010]** The present invention has been accomplished to go at least some way towards solving the above problems caused when the surface mount devices such as a semiconductor chip and a chip size package are mounted. The present invention provides a sheet of metal foil having bumps, a circuit substrate having the sheet of metal foil, and a semiconductor device having the circuit substrate capable of easily obtaining a mount structure in which the external connection terminals and the connection electrodes can be electrically connected with each other even when the external connection terminals, which are electrically connected to the electrode terminals, are formed on the electrode terminal carrying surface of the semiconductor chip.

**[0011]** According to this invention a sheet of metal foil having bumps is characterized in that the bumps, which are electrically connected to connection electrodes provided on one face of a surface mount device such as a semiconductor chip or a chip size package, are arranged in the same planar arrangement as that of said connection electrodes, and protrude from one side of said sheet of metal foil.

**[0012]** Also, the present invention provides a sheet of metal foil having bumps, wherein lands to which the external connection terminals are joined, which respectively correspond to the bumps, are formed on the other side of said sheet of metal foil.

[0013] Also, the present invention provides a sheet of metal foil having bumps, wherein wiring patterns are formed for electrically connecting the bumps to the lands, to which the external connection terminals are joined, and are supported on supporters which couple adjacent wiring patterns.

[0014] Also, the present invention provides a sheet of metal foil having bumps, wherein the external connection terminals respectively corresponding to the bumps are formed on the side of said sheet of metal foil opposite the bumps.

[0015] Also, the present invention provides a sheet of metal foil having bumps, wherein wiring patterns are formed for electrically connecting the bumps to the external connection terminals, and are supported on supporters which couple adjacent wiring patterns.

[0016] Also, the present invention provides a sheet of metal foil having bumps, wherein the external connection terminals are made of conductive material different from that of said sheet of metal foil.

[0017] Also, the present invention provides a sheet of metal foil having bumps, wherein an insulating adhesive agent layer is formed on one side of said sheet of metal foil.

[0018] Also, the present invention provides a sheet of metal foil having bumps, wherein tips of the bumps protrude from a surface of the insulating adhesive agent layer.

[0019] Also, the present invention provides a sheet of metal foil having bumps, wherein a charrier tape is adhered onto the other side of said sheet of metal foil.

[0020] Also, the present invention provides a circuit substrate of a single or multiple layer including a sheet of metal having bumps characterized in that the bumps, which are electrically connected to connection electrodes provided on one face of a surface mount device such as a semiconductor chip or a chip size package, are arranged in the same planar arrangement as that of said connection electrodes and protrude from one side of the sheet of metal foil on which wiring patterns, which are electrically connected to the bumps, are formed; and an insulating adhesive agent layer is adhered to one face of the sheet of metal foil having bumps.

[0021] Also, the present invention provides a circuit substrate of a single or multiple layer, wherein the wiring pattern is an island-shaped wiring pattern having a land to which an external connection terminal is joined at a base portion of the bump.

[0022] Also, the present invention provides a circuit substrate of a single or multiple layer, wherein the wiring pattern is a wiring pattern having a land to which the external connection terminal is joined on the other end side of the bump.

[0023] Also, the present invention provides a circuit substrate of a single or multiple layer characterized in that bumps, which are electrically connected to connection electrodes provided on one face of a surface mount device such as a semiconductor chip or a chip size pack-

age, are arranged in the same planar arrangement as that of said connection electrodes and protrude from one side of the sheet of metal foil; external connection terminals respectively corresponding to said bumps protrude from the other side of said sheet of metal foil; on which wiring patterns are formed for electrically connecting the bumps to said external connection terminals; and an insulating layer is adhered to said one side of the sheet of metal foil having bumps.

10 [0024] Also, the present invention provides a circuit substrate of a single or multiple layer, wherein the external connection terminals are made of conductive material different from that of the sheet of metal foil.

[0025] Also, the present invention provides a circuit substrate of a single or multiple layer, wherein the conductive material is made of conductive paste.

[0026] Also, the present invention provides a circuit substrate of a single or multiple layer, wherein tips of the bumps protrude from a surface of the insulating adhesive agent layer.

[0027] Also, the present invention provides a semi-

25 conductor device characterized in that a circuit substrate of a single or multiple layer which is composed in such a manner that bumps, which are electrically connected to connection electrodes provided on one face of a surface mount device such as a semiconductor chip or a chip size package, are arranged in the same planar arrangement as that of said connection electrodes and protrude from one side of the sheet of metal foil; on

30 which wiring patterns, which are electrically connected to said bumps, are formed; and an insulating adhesive agent layer is adhered to said one side of the sheet of metal foil having bumps, the insulating adhesive layer also adhered to said one face of the surface mount de-

[0028] Also, the present invention provides a semi-

[0022] Also, the present invention provides a semiconductor device, wherein the wiring pattern is an island-shaped wiring pattern having a land to which the external connection terminal is joined at a base portion of the bump.

[0029] Also, the present invention provides a semiconductor device, wherein the wiring pattern is a wiring pattern having a land to which the external connection terminal is joined on the other end side of the bumps.

- terminal is joined on the other end side of the bumps.

[0030] Also, the present invention provides a semiconductor device, wherein the external connection terminals are joined to the lands.

[0031] Also, the present invention provides a semi-

[0031] Also, the present invention provides a semiconductor device characterized in that a circuit substrate of a single or multiple layer which is composed in such a manner that, bumps, which are electrically connected to connection electrodes provided on one face of a surface mount device such as a semiconductor chip or a chip size package, are arranged in the same planar arrangement as that of said connection electrodes and protrude from one side of the sheet of metal foil; on which wiring patterns are formed for electrically con-

necting said bumps to external connection terminals; which respectively correspond to the bumps and protrude from the other side of the sheet of metal foil; and an insulating adhesive agent layer is adhered to said one face of the sheet of metal foil having bumps, the insulating adhesive layer also adhered to said one face of the surface mount device; and tips of the bumps respectively come into contact with the connection electrodes.

[0032] Also, the present invention provides a semiconductor device, wherein the outside of the external connection terminals are plated with solder.

[0033] Also, the present invention provides a semiconductor device, wherein the external connection terminals are made of conductive material different from that of the sheet of metal foil.

[0034] The sheet of metal foil having bumps, the circuit substrate having the sheet of metal foil, and the semiconductor device having the circuit substrate of the present invention can provide the following advantages. Even when the connection electrodes of the surface mount device such as a semiconductor chip or a chip size package are very densely arranged, it is possible to electrically connect the external connection terminals to the connection electrodes without extending the mount area.

[0035] The present invention can also provide the following advantages. Since bumps are formed on a sheet of metal foil by press working, the sheet of metal foil having the bumps according to the present invention can be suitably mass-produced, and the manufacturing cost can be reduced. Further, it is possible to easily make a circuit substrate having bumps arranged very densely.

[0036] Also, the present invention can provide the following advantages. The circuit substrate according to the present invention, which has the adhesive agent layer provided on the sheet of metal foil having bumps, can be made to adhere onto the electrode terminal carrying surface of the semiconductor chip. Therefore, the semiconductor device can be easily manufactured.

[0037] Further, the semiconductor device according to the present invention can be easily manufactured.

[0038] Furthermore, thermal stress generated by a difference of the coefficient of thermal expansion between the mount substrate and the semiconductor chip can be effectively reduced by the adhesive agent layer. Therefore, it is possible to conduct mounting very reliably.

[0039] Particular embodiments of this invention will now be described with reference to the accompanying drawings; in which:-

Fig. 1 is a cross-sectional view showing an embodiment of the semiconductor device;

Fig. 2 is a cross-sectional view showing another embodiment of the semiconductor device;

Fig. 3 is a cross-sectional view showing still another embodiment of the semiconductor device;

5

Fig. 4 is a cross-sectional view showing an embodiment of the sheet of metal foil having bumps;

Fig. 5 is a cross-sectional view showing another embodiment of the sheet of metal foil having bumps;

Fig. 6 is a cross-sectional view showing still another embodiment of the sheet of metal foil having bumps;

Fig. 7 is a cross-sectional view showing still another embodiment of the sheet of metal foil having bumps;

Fig. 8 is a plan view showing a plane arrangement of the bumps;

Fig. 9 is a plan view showing a plane arrangement of the bumps, lands and wiring patterns;

10

Figs. 10(a1) to 10(d2) are perspective views and cross-sectional views showing examples of the bumps;

20

Figs. 11(a1) to 11(d2) are perspective views and cross-sectional views showing another example of the bumps;

Figs. 12(a1) to 12(c) are perspective views and cross-sectional views showing still another example of the bumps;

25

Fig. 13 is a cross-sectional view showing an embodiment of the circuit substrate;

Fig. 14 is a cross-sectional view showing another embodiment of the circuit substrate;

Fig. 15 is a cross-sectional view showing still another embodiment of the circuit substrate;

Fig. 16 is a cross-sectional view showing still another embodiment of the circuit substrate;

Fig. 17 is a cross-sectional view showing still another embodiment of the circuit substrate;

Fig. 18 is a cross-sectional view showing an embodiment of the multi-layer circuit substrate;

30

Figs. 19(a1) to 19(c) are schematic illustrations showing a method of manufacturing the semiconductor device;

Fig. 20 is a cross-sectional view showing another embodiment of the semiconductor device;

35

Fig. 21 is a cross-sectional view showing still another embodiment of the semiconductor device; and

Fig. 22 is a schematic illustration showing an arrangement of the electrode terminals and lands of the semiconductor chip.

40

45

## SEMICONDUCTOR DEVICE

50

[0040] Figs. 1 to 3 are cross-sectional views respectively showing an arrangement of the semiconductor device manufactured by using a sheet of metal foil 20 having bumps.

55

[0041] Fig. 1 is a cross-sectional view showing a semiconductor device manufactured in such a manner that the sheet of metal foil 20 having bumps is made to adhere onto an electrode terminal carrying surface of the semiconductor chip 10 via the adhesive agent layer 18.

This sheet of metal foil 20 having bumps used for the semiconductor device is composed in such a manner that the bumps 22 are formed on the sheet of metal foil in the same plane arrangement as that of the electrode terminals 12 formed on the electrode terminal carrying surface. As shown in the drawings, the sheet of metal foil 20 having bumps is made to adhere onto the electrode terminal carrying surface of the semiconductor chip 10 via the adhesive agent layer 18 under the condition that each forward end portion of the bump 22 comes into contact with each electrode terminal 12.

[0042] On the sheet of metal foil 20, there are provided wiring patterns 26 for electrically connecting each bump 22 to each external connection terminal 24. The bump 22 is formed on one end side of the wiring pattern 26, and the land 28 for joining the external connection terminal 24 is formed on the other end side of it. In the embodiment shown in Fig. 1, solder balls are used for the external connection terminals 24. Each bump 22 is formed into a configuration, the size of which is minute, so that the bump 22 can be connected to the electrode terminal 12. On the other hand, the land 28 is formed into a configuration, the size of which is a predetermined value, so that the land 28 can be joined to an external connection terminal such as a solder ball.

[0043] In the above embodiment, the external surface of the sheet of metal foil 20 having bumps is covered with the protective film 30 of solder resist so that only the lands 28 can be exposed.

[0044] When the semiconductor device shown in Fig. 1 is mounted on a mount substrate, the external connection terminal 24 is joined to a connecting section of the circuit pattern provided on the mount substrate. The adhesive agent layer 18 has a function of making the sheet of metal foil 20 having bumps adhere to the semiconductor chip 10. Also, the adhesive agent layer 18 has a function of reducing thermal stress generated between the mount substrate and the semiconductor element 10.

[0045] In this connection, the semiconductor device may be composed in such a manner that the external connection terminal 24 is not joined to the land 28 but the land 28 is left being exposed and a connection bump provided on the mount substrate is joined to the land 28.

[0046] The semiconductor device shown in Fig. 2 is characterized in that both the bumps 22 and the external connection terminals 23 are previously formed on the sheet of metal foil. On the sheet of metal foil 20 having bumps, the protruding connection terminals 23 are formed by press working so that the protruding connection terminals 23 can agree with the positions of the connecting portions of the wiring patterns provided on the mount substrate. Each bump 22 is electrically connected to each connection terminal 23, so that the wiring pattern 26 can be formed.

[0047] When the connection terminals 23 are formed being protruded as shown in Fig. 2, the semiconductor device can be manufactured by positioning and solder-

ing the connection terminals 23 and the connecting sections of the mount substrate. In this connection, when the external faces of the connection terminals 23 are previously plated with solder, mounting can be easily carried out.

[0048] When the sheet of metal foil 20 having bumps, on which the protruding connection terminals 23 are formed as shown in Fig. 2, is used, it is possible to provide an advantage that mounting can be carried out without using the external connection terminals 24 such as solder balls. When the bumps 22 and the connection terminals 23 are formed on the sheet of metal foil by press working, the sheet of metal foil 20 having bumps can be manufactured at low cost.

[0049] Fig. 3 is a cross-sectional view showing still another embodiment of the semiconductor device. In this embodiment, the wiring patterns are not drawn around, and the lands 28 are provided in the same plane arrangement as that of the electrode terminals 12 of the semiconductor chips 10, and the external connection terminals 24 are joined to the lands 28. A base portion of each bump 22 is formed into an independent island-shape, and an external face of the base portion of the bump 22 is formed onto the land 28 to which the external connection terminal 24 is joined. Also, in this embodiment, each wiring pattern 26 is composed of the bump 22 and the land 28.

[0050] On the external face of the base portion of the bump 22, there is provided a recess which is formed when the bump 22 is formed into a protruding shape. This recess is filled with solder when the external connection terminal 24 such as a solder ball is joined to the recess. Except for the lands 28, the external face of the sheet of metal foil 20 having bumps is covered with a protective film 30 made of solder resist.

[0051] When the plane arrangement of the electrode terminals 12 and that of the external connection terminals 24 are made to be the same as shown in this embodiment, the bump 22 can be formed into a minute configuration so that it can be connected to the electrode terminal 12, and on the other hand, the land 28 is provided with a necessary area so that it can be joined to the external connection terminal 24. Therefore, the bump 22 and the land 28 have a function of converting the size of the electrode terminal 12 into the size of the external connection terminal 24. The aforementioned function of converting the size of the electrical connecting section is useful, because it becomes possible to connect a larger external connection terminal 24 to the land 28 in the same arrangement even when the electrode terminal 12 is formed into a minute configuration. Since the adhesive agent layer 18 is interposed in this embodiment, it is possible to reduce thermal stress generated in the case of mounting.

[0052] In the semiconductor devices of the aforementioned embodiments shown in Figs. 1 to 3, the bumps 22 on the sheet of metal foil are connected to the electrode terminals 12 provided on the electrode terminal

carrying surface of the semiconductor chip 10. However, it is possible to adopt an arrangement in which the bumps 22 are connected to the connection electrodes formed by rewiring on the electrode terminal carrying surface of the semiconductor chip 10.

[0053] Rewiring is conducted in the case where the electrode terminals 12 are very densely arranged, so that the bumps 22 can not be connected to the electrode terminals 12 as they are. Also, rewiring is conducted in the case where the connection electrodes for connecting the bumps 22 are arranged according to the arrangement of the external connection terminals 24. In the case of the semiconductor chip 10 in which the connection terminal is formed by rewiring on the electrode terminal carrying surface, it is possible to provide a semiconductor device capable of being mounted when the sheet of metal foil 20 having bumps is made to adhere by the adhesive agent layer 18 and the bumps 22 are connected to the connection electrodes.

#### SHEET OF METAL FOIL HAVING BUMPS

[0054] Figs. 4 to 7 are views showing embodiments of the sheet of metal foil having bumps.

[0055] Fig. 4 is a view showing a sheet of metal foil 20, on one face 20a of which the bumps 22 are formed in the same arrangement as that of the electrode terminals of the connection electrodes provided on the surface mount device such as a semiconductor chip 10 or a chip size package.

[0056] On this sheet of metal foil 20 having bumps, the protruding bumps 22 are formed when a flat sheet of metal foil 20a is subjected to press working. The method of forming the bumps 22 by press working is advantageous in that a large number of bumps 22 can be effectively formed, so that the sheets of metal foil 20 having bumps can be easily manufactured and mass-produced.

[0057] Fig. 8 is a view showing an example of the plane arrangement of the bumps 22 provided on the sheet of metal foil. The bumps 22 are formed according to the arrangement of the connection electrodes such as the electrode terminals 12 formed on the electrode terminal carrying surface of the semiconductor chip 10. For example, when the electrode terminals 12 are arranged in the shape of an area array, the bumps 22 are also arranged in the shape of an area array as shown in the drawing.

[0058] The configuration of each bump 22 formed on the sheet of metal foil may be a configuration by which the bump 22 can be contacted with and electrically connected to the connection electrode provided on surface mount device such as a semiconductor chip or a chip size package.

[0059] Fig. 4 is a view showing an example of the sheet of metal foil 20 having bumps which are formed conical. However, it is possible to form the bumps 22 into various configurations. Figs. 10 to 12 are perspec-

tive and cross-sectional views of the bumps 22 formed on the sheet of metal foil. Figs. 10(a1) to 10(d2) are views showing examples of the configurations of the bumps 22 which are formed into a cone, pyramid, hemisphere and column. Figs. 11(a1) to 11(d2) are views showing configurations of the bumps 22 which are raised by cutting. In these examples, the side configurations are formed into a V-shape, U-shape, J-shape and L-shape. Figs. 12(a1) to 12(b2) are views of the configurations of the bumps, the side configurations of which are formed by combining two J-shape components opposed to each other and also by combining two sharp J-shape components opposed to each other. Fig. 12(c) is a view showing an example of the configuration of the bump which is formed into a spiral.

[0060] As shown in Figs. 10(a1) to 10(c2), when the bump 22 is formed into a cone, pyramid or hemisphere, the configuration of the bump 22 can be stably maintained, and the positional accuracy can be enhanced. The bump 22 having a top in the configuration, such as the conical bump 22, is superior to the columnar bump 22 shown in Figs. 10(d1) and 10(d2), because it is possible for the bump 22 having the top to conduct electrical connection by point contact, so that the connection electrodes can be very densely arranged, that is, the bump 22 having the top, including such as the conical bump 22, can be easily joined to the connection electrode. In this connection, in the examples shown in Figs. 10(a1) to 10(d2), it is possible to form a through-hole at the top of the bump 22.

[0061] When the bumps 22 are formed by being raised by cutting as shown in Figs. 11 and 12, the sides of the bumps 22 are open. Especially, in the cases shown in Figs. 11(c1) and 11(c2) and also shown in Figs. 11(d1) and 11(d2), in which the bumps 22 are formed into a J-shape, L-shape or sharp J-shape and one of the base portions supporting the bump 22 is separate from the sheet of metal foil, elasticity is given to the bump 22. Due to the elasticity of the bump 22, thermal stress generated in the process of mounting on a mount substrate can be reduced by the bump 22. In the case of the spiral bump 22 shown in Fig. 12(c), the elasticity and cushioning function of the bump 22 can be further enhanced, and thermal stress can be more effectively reduced.

[0062] The sheet of metal foil 20 having bumps can be made of metal such as copper, aluminum, gold, silver or stainless steel. When the bumps 22 are formed on the sheet of metal foil 20a by press working, the prior art of press working in which a die and punch are used can be applied. When a metal sheet is subjected to press working, it is possible to provide a very high accuracy of forming. Therefore, minute bumps 22 can be easily formed according to the arrangement of the connection electrodes. In this connection, in the case where the bumps 22 are formed on the sheet of metal foil 20a, it is possible to form the bumps 22 of the same configuration on the overall sheet of metal foil 20a. It is also possible to form bumps 22 of different configurations

which are arranged on the sheet of metal foil 20a being mixed with each other.

[0063] Fig. 5 is a view showing a sheet of metal foil 20 having both the bumps 22 and the connection terminals 23 used as external connection terminals. That is, on the sheet of metal foil 20a, the bumps 22 and the connection terminals 23 are formed by press working. Since the connection terminals 23 are used as external connection terminals, they are formed being protruded onto the opposite side to the side on which the bumps 22 are formed on the sheet of metal foil 20a. As shown in Figs. 10 to 12, the connection terminals 23 may be formed into various configurations. However, since the connection terminals 23 are connected to the connecting sections of the mount substrate by solder, it is preferable that the configuration of each connection terminal 23 is formed so that a predetermined joining area can be ensured.

[0064] In this connection, instead of forming the connection terminals 23 by press working, a conductor having bumps, which is different from the sheet of metal foil 20a, may be formed on the face of the sheet of metal foil 20a onto which the external connection terminals are connected, so that the conductor can be used as the connection terminals 23. Examples of the methods of forming the connection terminals 23 by the different conductor are: a method in which the connection terminals are made to swell by plating; and a method in which the connection terminals are formed into bumps by printing or transferring conductor paste.

[0065] When the above sheet of metal foil 20 having bumps provided with the external connection terminals 23 is used, it becomes unnecessary to join the external connection terminals such as solder balls in the later process.

[0066] The sheet of metal foil 20 shown in Figs. 6 and 7 is characterized in that the wiring patterns 26 for electrically connecting the bumps 22 with the external connection terminals are formed. Fig. 9 is a view showing the wiring patterns 26 including the bumps 22 and the lands 28. Each wiring pattern 26 is formed being drawn around on a plane so that the bump 22 and the land 28, to which the external terminal is joined, can be electrically connected with each other. In order to independently form the bump 22, the land 28 and the wiring pattern 26 for connecting them, it is preferable that the wiring pattern 26 is supported by the carrier tape 32 capable of being peeled off from the sheet of metal foil 20a as shown in Fig. 6.

[0067] Fig. 7 is a view showing a sheet of metal foil 20 having bumps on which the wiring patterns 26 for connecting the bumps 22 to the connection terminals 23 are formed. In the case of this sheet of metal foil 20 having bumps, the wiring patterns 26 can be connected to and supported by the support frame without using the above carrier tape 32.

[0068] In this connection, in the case where the bumps 22 are formed by press working on the sheet of

metal foil 20a, it is possible to form the bumps 22 after the sheet of metal foil 20a has been patterned.

#### CIRCUIT SUBSTRATE

[0069] As shown in Figs. 1 to 3, the sheet of metal foil 20 having bumps can be attached onto the electrode terminal carrying surface of the semiconductor chip 10 or the electrode terminal carrying surface of the surface mount device such as a chip size package. In this way, the sheet of metal foil 20 having bumps can be used for composing a predetermined mount structure of the semiconductor device.

[0070] When the sheet of metal foil 20 having bumps is attached to the electronic device such as a semiconductor chip 10 as described above, it is attached via the adhesive agent layer 18. Therefore, it is effective to previously provide the adhesive agent layer 18 on the sheet of metal foil 20 having bumps.

[0071] Figs. 13 to 16 are views showing examples of the sheet of metal foil 20 having bumps on which the adhesive agent layer 18 is provided.

[0072] Fig. 13 is a view showing the sheet of metal foil 20 having bumps, on one face of the sheet of metal foil 20a of which the protruding bumps 22 are formed and the adhesive agent layer 18 is provided. In this case, the adhesive agent layer 18 is provided so that all of the one face of the sheet of metal foil 20 having bumps can be covered with the adhesive agent layer 18. In this connection, in the case where one face of the sheet of metal foil 20 having bumps on which the bumps 22 are formed is covered with the adhesive agent layer 18 and the tip portions of the bumps 22 are protruded from the surface of the adhesive agent layer 18, the following two cases may be encountered. One is a case in which the tip portions of the bumps 22 and the surface of the adhesive agent layer 18 are made to be on the same face, and the surfaces of the bump 22 are exposed from the surface of the adhesive agent layer 18. The other is a case, the tip portions of the bumps 22 are embedded in the adhesive agent layer 18.

[0073] In the case where the tip portions of the bumps 22 are protruded or exposed from the adhesive agent layer 18, the sheet of metal foil 20 having bumps can be electrically connected to the connection electrodes such as the electrode terminals 12 provided in the electronic part such as the semiconductor chip 10 as they are.

[0074] Even if the bumps 22 are embedded in the adhesive agent layer 18, when the sheet of metal foil 20 having bumps is made to adhere onto the adhesive face while they are being strongly pressed against the adhesive face, the tip portions of the bumps 22 can be protruded from the adhesive agent layer 18, so that the tip portions of the bumps 22 can be pressed against the connection electrodes such as the electrode terminals 12. In this way, the electrical connection can be accomplished.

[0075] Fig. 14 is a view showing an embodiment of

the sheet of metal foil 20 having bumps on which the bumps 22 and the connection terminals 23 are provided, and the adhesive agent layer 18 is provided on the face of the sheet of metal foil 20 on which the bumps 22 are formed.

[0076] Fig. 15 is a view showing a circuit substrate 40 which has the adhesive agent layer 18 covering the bump carrying face of the sheet of metal foil 20 having bumps on which the wiring patterns 26 are formed.

[0077] Fig. 16 is a view showing a circuit substrate 40 which has the adhesive agent layer 18 provided on the sheet of metal foil 20 having bumps on which the bumps 22, the connection terminals 23 and the wiring patterns 26 for electrically connecting them are formed. When the wiring patterns 26 are formed, the wiring patterns for electrically connecting the bumps 22 to the connection terminals 23 can be used as signal patterns, ground patterns or power supply patterns.

[0078] In this connection, in this specification, the circuit substrate 40 is defined as a sheet of metal foil 20 having bumps provided with the adhesive agent layer 18 on which the wiring patterns 26 are formed on the sheet of metal foil 20a. Also, in this specification, the sheet of metal foil having bumps is defined as a sheet of metal foil 20 having bumps in which only bumps 22 are formed on the sheet of metal foil 20a and no wiring patterns 26 are formed.

[0079] Concerning the form of the sheet of metal foil 20 having bumps provided with the adhesive agent layer 18 and also concerning the form of the circuit substrate 40, it is possible to adopt various forms as described before according to the configurations of bumps 22 provided on the sheet of metal foil 20 having bumps, the configurations of the connection terminals 23, and/or the wiring patterns 26. As long as a predetermined adhesion function can be provided by the adhesive agent layer 18 adhering to the sheet of metal foil 20 having bumps, any adhesive agent layer 18 may be adopted. Either thermosetting resin or thermoplastic resin may be used, that is, the material is not particularly restricted.

[0080] As shown by the embodiments illustrated in Figs. 13 and 14, the sheet of metal foil 20 having bumps and the circuit substrate 40 may be provided in such a manner that all face on the mount face side is exposed. Alternatively, as shown by the embodiments illustrated in Figs. 15 and 16, the sheet of metal foil 20 having bumps and the circuit substrate 40 may be provided in such a manner that the mount face side is covered with the protective film 30 made of solder resist. In the case where the mount face side of the circuit substrate 40 is covered with the protective film 30, the lands 28 to which the external connection terminals are joined are exposed, or the connection end portions of the connection terminals 23 are exposed.

[0081] On the circuit substrate 40, it is preferable that the connection end portions of the lands 28 with the connection terminals 23 are plated by nickel-gold alloy so that the connection end portions can be excellently

joined to the external connection terminals. In the case of plating by nickel-gold alloy, the mount face side of the sheet of metal foil 20a may be covered with the protective layer 30 made of solder resist, and electrolytic plating may be conducted under this condition.

[0082] On the sheet of metal foil 20 having bumps provided with the adhesive agent layer 18 and also on the circuit substrate 40, the tip portions of the bumps 22 exposed onto the surface of the adhesive agent layer 18 may be subjected to plating of gold, tin, lead or silver, or alternatively the tip portions of the bumps 22 exposed onto the surface of the adhesive agent layer 18 may be coated with conductive material such as silver paste, so that the tip portions of the exposed bumps 22 can be electrically connected with the connection electrodes provided in the electronic part such as a semiconductor chip.

#### METHOD OF MANUFACTURING THE CIRCUIT SUBSTRATE AND OTHERS

[0083] Methods of manufacturing the above circuit substrate 40 and the sheet of metal foil 20 having bumps provided with the adhesive agent layer 18 are divided into two main methods. One is a method in which, before a predetermined wiring pattern is formed on the sheet of metal foil 20a, one face, on which the bumps are formed, of the sheet of metal foil 20a is covered with the adhesive agent layer 18. The other is a method in which, after a predetermined wiring pattern has been formed on the sheet of metal foil 20a, one face of the sheet of metal foil 20a is covered with the adhesive agent layer 18.

[0084] The method in which one face, on which the bumps are formed, of the sheet of metal foil 20a is covered with the adhesive agent layer 18 before a predetermined wiring pattern is formed on the sheet of metal foil 20a, is divided into the following two methods (1) and (2).

[0085] Method (1) is described as follows. The sheet of metal foil 20a is subjected to press working so as to form the bumps 22. After that, the face on which the bumps 22 have been formed are covered with the adhesive agent layer 18. Then, the wiring patterns are formed.

[0086] On the sheet of metal foil 20 having bumps provided with the adhesive agent layer shown in Fig. 13, when the sheet of metal foil 20a is etched, it is possible to obtain the circuit substrate 40 having the wiring pattern 26 shown in Fig. 17. Since the sheet of metal foil 20a is supported by the adhesive agent layer 18, it is possible to form an arbitrary wiring pattern.

[0087] The sheet of metal foil 20 having bumps shown in Fig. 13, on which the wiring patterns have not been formed yet, can be made by the following methods. One is a method in which liquid of insulating resin, which becomes the adhesive agent layer 18, is coated on the sheet of metal foil 20a on which the bumps 22 are

formed. The other is a method in which an adhesive agent sheet having a function of adhesion is made to adhere.

**[0088]** As described above, the tip portions of the bumps 22 are exposed onto the surface of the adhesive agent layer 18 or embedded in the adhesive agent layer 18. In order to expose the tip portions of the bumps 22 from the surface of the adhesive agent layer 18, after liquid resin is coated on the surface of the sheet of metal foil 20a, or alternatively after the adhesive agent sheet is made to adhere, a pressing jig having a flat face is pressed on the adhesive agent layer 18 in the thickness direction of it, so that the tip portions of the bumps 22 can be exposed onto the surface of the adhesive agent layer 18. If the pressing jig is made of material having a cushioning function and also if the surface of the pressing jig for pressing the adhesive agent layer 18 is made to be separable, it becomes possible to protrude the tip portions of the bumps 22 from the surface of the adhesive agent layer 18. In this connection, when pressing is conducted by the pressing jig, the adhesive agent layer 18 may be heated a little so as to ensure the configuration.

[0089] Method (2) is described as follows. After the adhesive agent layer 18 has been made to adhere onto one face of the sheet of metal foil 20a, the bumps 22 are formed, and then the wiring patterns are formed.

[0090] According to this method, when the bumps 22 are formed by press working on the sheet of metal foil 20a, the bumps 22 are formed via the adhesive agent layer 18. At this time, simultaneously when the bumps 22 are formed, the tip portions of the bumps 22 are exposed from the adhesive agent layer 18.

**[0091]** In this connection, when the sheet of metal foil 20a is subjected to press forming, it is possible to form a predetermined wiring pattern before the bumps 22 are formed. Since the sheet of metal foil 20a is supported by the adhesive agent layer 18, the predetermined wiring pattern may be formed on the sheet of metal foil 20a either before or after the bumps 22 are formed.

[0092] After the predetermined wiring pattern has been formed on the sheet of metal foil 20a, one face of the sheet of metal foil 20a is covered with the adhesive agent layer 18. In this case, the following methods (3) to (5) are provided.

[0093] Method (3) is described as follows. After the predetermined wiring patterns have been formed on the sheet of metal foil 20a and the bumps 22 have been formed, the bump carrying face is covered with the adhesive agent layer 18. According to this method, the pre-determined wiring patterns are formed on the sheet of metal foil 20a under the condition that the adhesive agent layer 18 has not been formed. Therefore, it is necessary to form the wiring pattern while the sheet of metal foil 20a is being supported by the frame. After the wiring patterns 26, the configurations of which are established by themselves, have been formed as described above, liquid of insulating resin is coated on the bump carrying

face, or alternatively an adhesive agent sheet is made to adhere, so that the adhesive agent layer 18 is provided. In this connection, the order of the process in which the predetermined wiring pattern is formed on the sheet of metal foil 20a and the process of forming the bumps 22 can be changed. Accordingly, it is possible to form the predetermined wiring patterns after the bumps 22 have been formed.

[0094] Method (4) is described as follows. After the predetermined wiring patterns have been formed on the sheet of metal foil 20a, one face of the sheet of metal foil 20a is covered with the adhesive agent layer 18, and press working is conducted on the sheet of metal foil 20a onto which the adhesive agent layer 18 is attached, so that the bumps 22 can be formed. According to this method, the predetermined wiring patterns are formed before the sheet of metal foil 20a is supported by the adhesive agent layer 18. Therefore the wiring patterns, which are adjacent to each other, must be connected to with each other by a support piece.

**[0095]** Since the adhesive agent layer 18 is attached onto the sheet of metal foil 20a, the sheet of metal foil 20a is subjected to press working via the adhesive agent layer 18, so that the bumps 22 can be formed. At this time, the tip portions of the bumps 22 are exposed or embedded in the adhesive agent layer 18.

[0096] In this connection, in the case where the predetermined wiring patterns are formed on the sheet of metal foil 20a before the sheet of metal foil 20a is supported by the adhesive agent layer 18 as described above, the wiring patterns, which are adjacent to each other, must be connected to with each other by a support piece. However, when the sheet of metal foil 20a is previously supported by the carrier tape 32, it becomes possible to form arbitrary wiring patterns on the sheet of metal foil 20a.

[0097] Method (5) is described as follows. The carrier tape 32 is made to adhere onto a face of the sheet of metal foil 20a opposite to the face on which the bumps 22 are formed, so that the sheet of metal foil 20a can be supported. Under the above condition, the predetermined patterns are formed on the sheet of metal foil 20a, or alternatively press working is conducted.

[0098] In the method of supporting the sheet of metal foil 20a by the carrier tape 32, either the formation of predetermined patterns on the sheet of metal foil 20a or the press working may be conducted first. That is, after the wiring patterns 26 and the bumps 22 have been formed by forming the predetermined patterns on the sheet of metal foil 20a and conducting press working, the adhesive agent layer 18 is made to adhere onto the face on which the bumps 22 are formed.

**[0099]** As an alternative method, the predetermined wiring patterns are formed on the sheet of metal foil 20a under the condition that the sheet of metal foil 20a is supported by the carrier tape 32, and the adhesive agent layer 18 is provided on one face of the sheet of metal foil 20a, and then the bumps 22 are formed by press

working.

[0100] The carrier tape 32 is provided for supporting the sheet of metal foil 20a. Therefore, the carrier tape 32 is selected so that it can be easily peeled off from the sheet of metal foil 20a. In the case of mounting, the carrier tape 32 is peeled off from the circuit substrate 40. In this connection, it is possible to adopt an arrangement in which the carrier tape 32 is made to adhere onto the face on which the adhesive agent layer 18 is provided or the mount face of the sheet of metal foil 20a in such a manner that the carrier tape 32 is separable so that it can be used for protecting the circuit substrate.

#### MULTILAYER CIRCUIT SUBSTRATE

[0101] All of the aforementioned circuit substrates are composed of a single layer. However, it is possible to provide a multilayer circuit substrate by laminating circuit substrates 40 on which the adhesive agent layers 18 are provided on the faces on which the bumps 22 are formed.

[0102] Fig. 18 is a view showing an embodiment of the multilayer circuit substrate. The circuit substrates 40 having the same wiring patterns 26 as those of the circuit substrate shown in Fig. 17 are laminated and adhere to each other by the adhesive agent layers 18, so that the multilayer circuit substrate can be obtained. The bumps 22 formed on the circuit substrate 40 function as vias for electrically connecting the wiring patterns 26 between the layers, and when the wiring patterns 26 and the bumps 22 on the layers are appropriately arranged, it is possible to obtain a multilayer circuit substrate having a predetermined electrical connection pattern.

[0103] In the case where the circuit substrates 40 are laminated so as to form a multiple layer, it is common that the tip portions of the bumps 22 on the lower layer come into contact to the lower face of the wiring patterns 26 on the upper layer. However, depending upon a case, the bumps 22 on the lower layer and the bumps 22 on the upper layer may be located at the same positions on a plane. When there is a possibility that an electrical connection can not be positively accomplished between the layers because of recesses formed at the bottom portions of the bumps 22 on the upper layer, the recesses of the bumps 22 may be filled with conductive material so as to ensure the electrical connection.

[0104] When the circuit substrate 40 having a multiple layer is provided, it is possible to accomplish various arrangements which can not be provided by the circuit substrate of a single layer. For example, it is possible to provide a ground layer or a power supply layer on the circuit substrate.

[0105] Concerning the configurations of the bumps 22 provided on the circuit substrate 40 laminated into a multiple layer, it is possible to use various forms combined with each other as shown in Figs. 10, 11 and 12.

#### METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES

[0106] The adhesive agent layer 18 is previously formed on the above circuit substrate 40 of a single or multiple layer, and the bumps 22 are formed according to the arrangement of the connection electrodes provided in the electronic device such as a semiconductor chip or a chip size package. Therefore, when the semiconductor device is manufactured, the electrode terminal carrying surfaces of the semiconductor chip 10 and the bumps 22 of the circuit substrate 40 are positioned so as to agree with each other and made to adhere by the adhesive agent layer 18. Due to the foregoing, the bumps 22 and the electrode terminals 12 can be electrically connected to with each other. In this way, it is possible to manufacture a semiconductor device having the wiring patterns 26 used for external connection and the lands 28 on the electrode terminal carrying surfaces.

[0107] Figs. 19(a1) to 19(c) are views showing a method by which the semiconductor device 50 is formed by making the circuit substrate 40 adhere to the semiconductor chip 10. The semiconductor chip 10 and the circuit substrate 40 are positioned with each other as shown in Figs. 19(a1) and 19(a2), and the circuit substrate 40 is made to adhere to the semiconductor chip 10 as shown in Fig. 19(b). Then, the external connection terminals 24 such as solder balls are joined to the lands 28. In this way, the semiconductor device 50 can be made as shown in Fig. 19(c).

[0108] In this connection, it is possible to use the semiconductor device 50 while the external connection terminals 24 are not joined. In the case of the circuit substrate 40 provided with the connection terminals 23, it is possible to use it as the semiconductor device 50 as it is. Also, in the case of the circuit substrate 40 provided with the connection terminals 23, solder bumps may be attached to the connection terminals 23.

[0109] The semiconductor device 50 is not limited to the face-down type shown in Fig. 19, but it is possible to adopt the face-up type shown in Fig. 20. Reference numeral 42 is a lead extending from the periphery of the electrode terminal carrying surface of the semiconductor chip 10. The lead 42 is bent so that it can be connected with the connecting section of the mount substrate.

[0110] Fig. 21 is a view showing a semiconductor device in which two semiconductor chips 10 are laminated on each other by using a multilayer circuit substrate. Electrode terminal carrying surfaces of the semiconductor elements 10, 10 are opposed to each other, and the adhesive agent layers 18 of the multilayer circuit substrate are made to adhere onto the electrode terminal carrying surfaces of the semiconductor chips 10, 10. Due to the foregoing, it is possible to obtain a semiconductor device in which the electrode terminals 12 of the semiconductor chips 10, 10 are electrically connected to the lead 42.

**Claims**

1. A sheet of metal foil having bumps characterized in that the bumps, which are electrically connected to connection electrodes provided on one face of a surface mount device such as a semiconductor chip or a chip size package, are arranged in the same planar arrangement as that of said connection electrodes, and protrude from one side of said sheet of metal foil.
2. A sheet of metal foil having bumps according to claim 1, wherein lands to which external connection terminals are joined, which respectively correspond to the bumps, are formed on the other side of said sheet of metal foil.
3. A sheet of metal foil having bumps according to claim 2, wherein wiring patterns are formed for electrically connecting the bumps to the lands, to which the external connection terminals are joined, and are supported on supporters which couple adjacent wiring patterns.
4. A sheet of metal foil having bumps according to claim 1, wherein the external connection terminals respectively corresponding to the bumps are formed on the side of said sheet of metal foil opposite the bumps.
5. A sheet of metal foil having bumps according to claim 4, wherein wiring patterns are formed for electrically connecting the bumps to the external connection terminals, and are supported on supporters which couple adjacent wiring patterns.
6. A sheet of metal foil having bumps according to claim 4 or claim 5, wherein the external connection terminals are made of conductive material different from that of said sheet of metal foil.
7. A sheet of metal foil having bumps according to any one of the preceding claims, wherein an insulating adhesive agent layer is formed on one side of said sheet of metal foil.
8. A sheet of metal foil having bumps according to claim 7, wherein tips of the bumps protrude from a surface of the insulating adhesive agent layer.
9. A sheet of metal foil having bumps according to any one of the preceding claims, wherein a carrier tape is adhered to the other side of said sheet of metal foil.
10. A circuit substrate of a single or multiple layer including a sheet of metal foil having bumps characterized in that the bumps, which are electrically con-

- 5 nected to connection electrodes provided on one face of a surface mount device such as a semiconductor chip or a chip size package, are arranged in the same planar arrangement as that of said connection electrodes and protrude from one side of the sheet of metal foil on which wiring patterns, which are electrically connected to said bumps, are formed; and an insulating adhesive agent layer is adhered onto one face of said sheet of metal foil having bumps.
- 10
11. A circuit substrate of a single or multiple layer according to claim 10, wherein the wiring pattern is an island-shaped wiring pattern having a land to which an external connection terminal is joined at a base portion of the bumps.
  - 15
  12. A circuit substrate of a single or multiple layer according to claim 10, wherein the wiring pattern is a wiring pattern having a land to which the external connection terminal is joined on the other end side of the bump.
  - 20
  13. A circuit substrate of a single or multiple layer characterized in that bumps, which are electrically connected to connection electrodes provided on one face of a surface mount device such as a semiconductor chip or a chip size package, are arranged in the same planar arrangement as that of said connection electrodes and protrude from one side of the sheet of metal foil; external connection terminals respectively corresponding to said bumps protrude from the other side of said sheet of metal foil; on which wiring patterns are formed for electrically connecting the bumps to said external connection terminals; and an insulating layer is adhered to said one side of the sheet of metal foil having bumps.
  - 25
  14. A circuit substrate of a single or multiple layer according to claim 13, wherein the external connection terminals are made of conductive material different from that of the sheet of metal foil.
  - 30
  15. A circuit substrate of a single or multiple layer according to claim 14, wherein the conductive material is made of conductive paste.
  - 35
  16. A circuit substrate of a single or multiple layer according to any one of claims 10 to 15, wherein tips of the bumps protrude from a surface of the insulating adhesive agent layer.
  - 40
  17. A semiconductor device characterized in that a circuit substrate of a single or multiple layer which is composed in such a manner that bumps, which are electrically connected to connection electrodes provided on one face of a surface mount device such as a semiconductor chip or a chip size package, are
  - 45
  - 50
  - 55

arranged in the same planar arrangement as that of said connection electrodes and protrude from one side of the sheet of metal foil; on which wiring patterns, which are electrically connected to said bumps, are formed; and an insulating adhesive agent layer is adhered on said one side of the sheet of metal foil having bumps, the insulating adhesive agent layer also adhering to said one face of the surface mount device; and tips of the bumps respectively come into contact with the connection electrodes.

5

10

18. A semiconductor device according to claim 17, wherein the wiring pattern is an island-shaped wiring pattern having a land to which the external connection terminal is joined at a base portion of the bump. 15
19. A semiconductor device according to claim 17, wherein the wiring pattern is a wiring pattern having a land to which the external connection terminal is joined on the other end side of the bump. 20
20. A semiconductor device according to any one of claims 17 to 19, wherein the external connection terminals are joined to the lands. 25
21. A semiconductor device characterized in that a circuit substrate of a single or multiple layer which is composed in such a manner that bumps, which are electrically connected to connection electrodes provided on one face of a surface mount device such as a semiconductor chip or a chip size package, are arranged in the same planar arrangement as that of said connection electrodes and protrude from one side of the sheet of metal foil; on which wiring patterns are formed for electrically connecting said bumps to external connection terminals which respectively correspond to the bumps and protrude from the other side of the sheet of metal foil; and an insulating adhesive agent layer is adhered to said one face of the sheet of metal foil having bumps, the insulating adhesive layer also adhering to said one face of the surface mount device; and tips of the bumps respectively come into contact with the connection electrodes. 30  
35  
40  
45
22. A semiconductor device according to claim 21, wherein the outside of the external connection terminals are plated with solder. 50
23. A semiconductor device according to claim 21 or claim 22, wherein the external connection terminals are made of conductive material different from that of the sheet of metal foil. 55

Fig.1

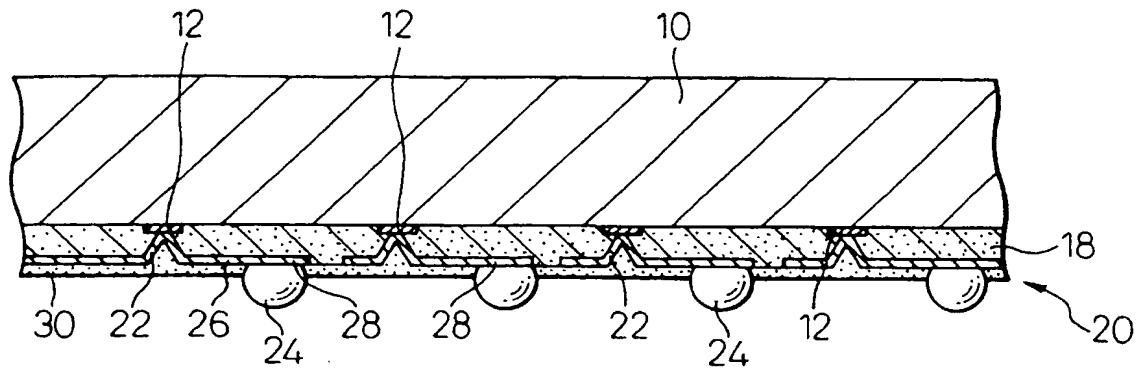


Fig.2

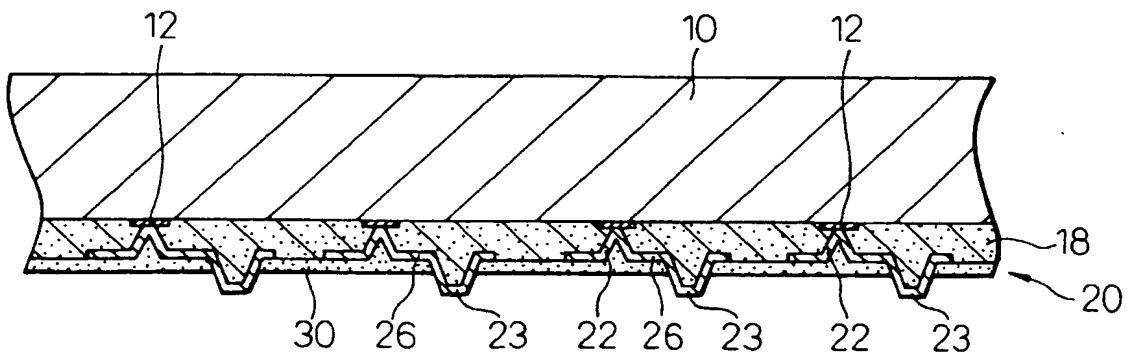


Fig.3

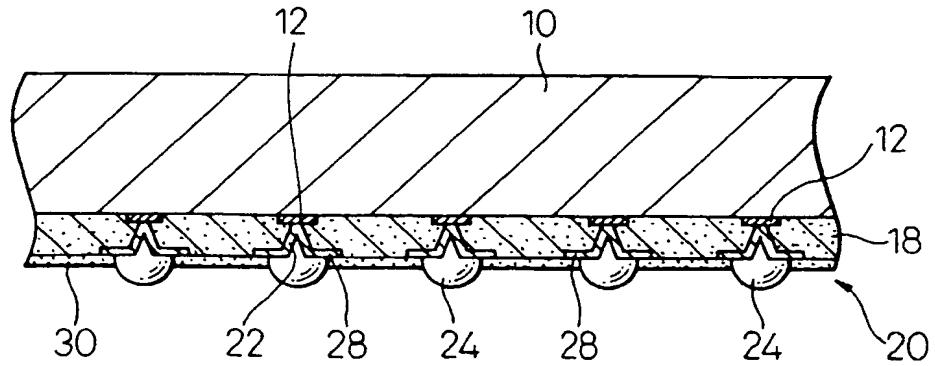


Fig.4

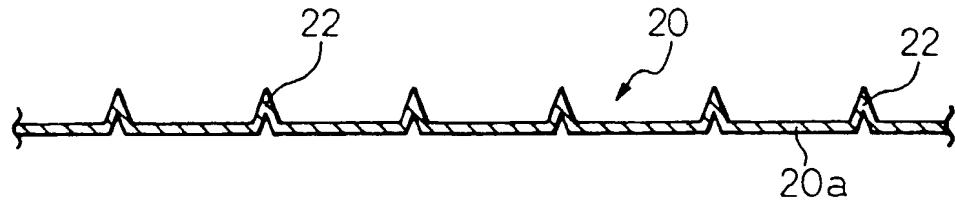


Fig.5

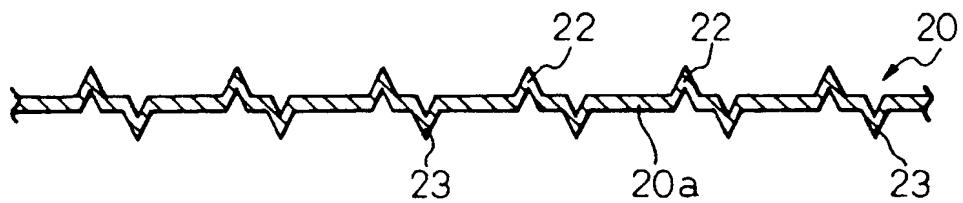


Fig.6

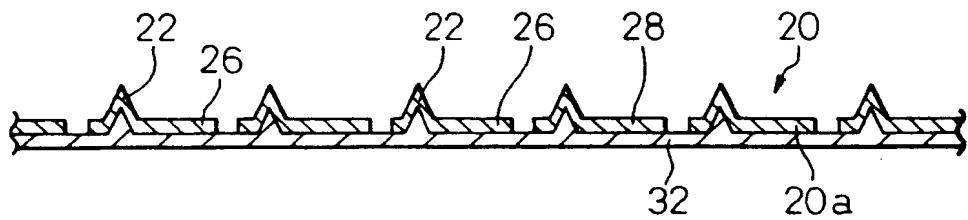


Fig.7

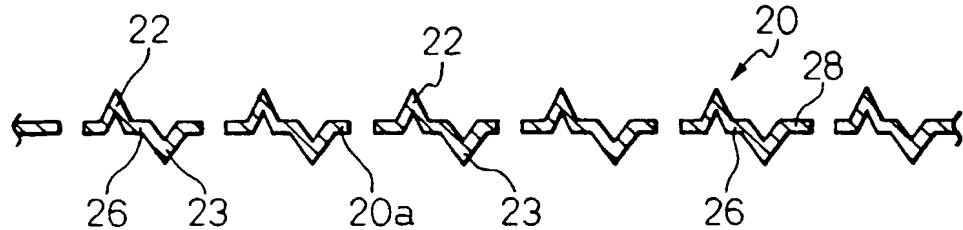


Fig.8

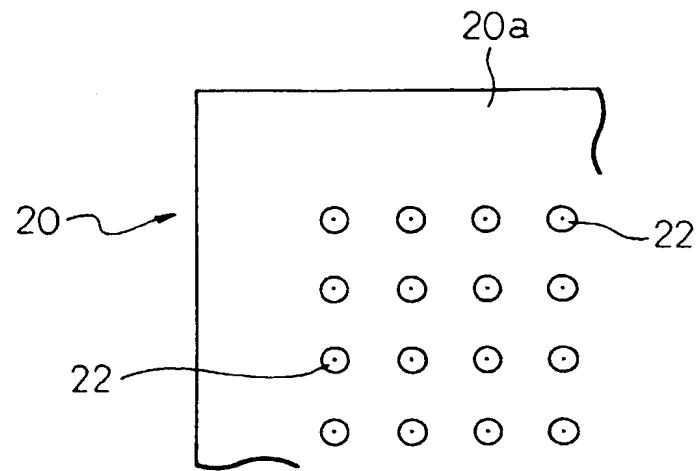


Fig.9

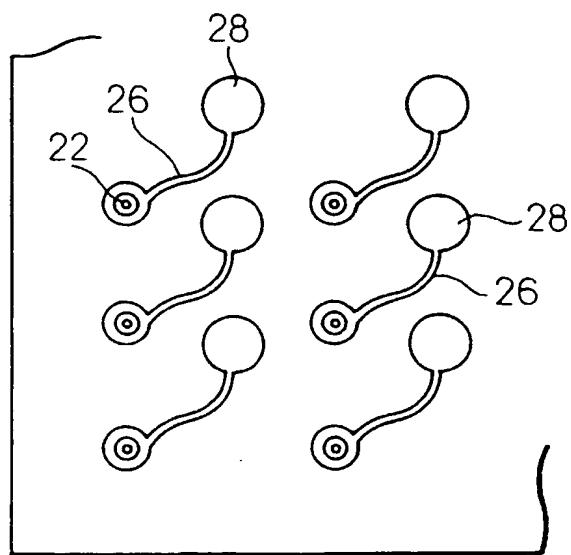


Fig.10(a1)

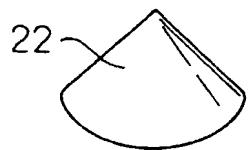


Fig.10(a2)

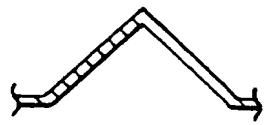


Fig.10(b1)

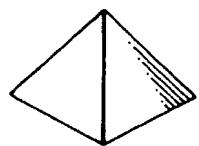


Fig.10(b2)

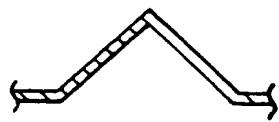


Fig.10(c1)

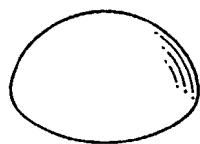


Fig.10(c2)

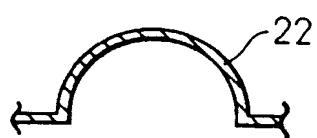


Fig.10(d1)

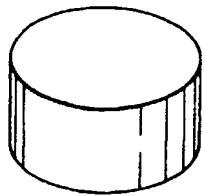


Fig.10(d2)



Fig.11(a1)

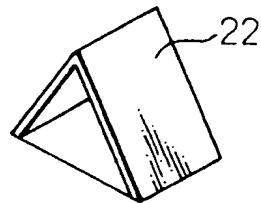


Fig.11(a2)

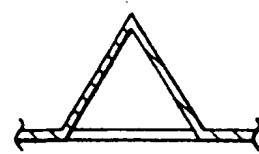


Fig.11(b1)

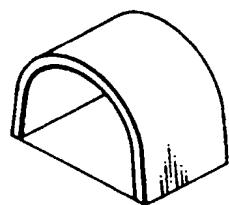


Fig.11(b2)

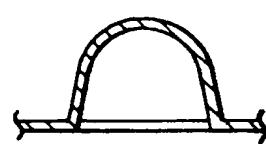


Fig.11(c1)

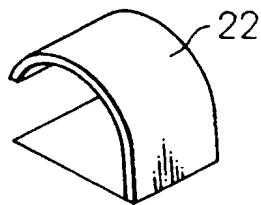


Fig.11(c2)

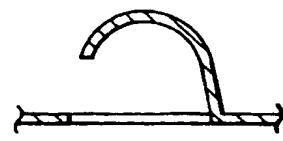


Fig.11(d1)

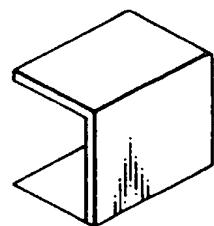


Fig.11(d2)

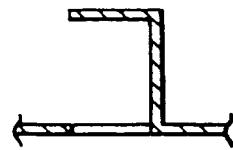


Fig.12(a1)

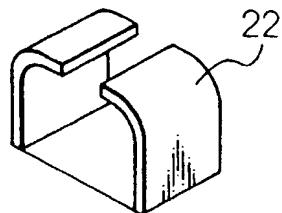


Fig.12(a2)

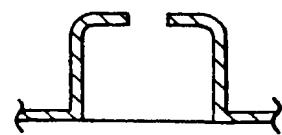


Fig.12(b1)

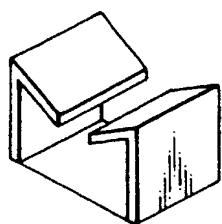


Fig.12(b2)

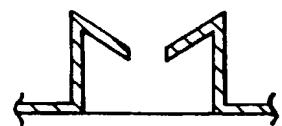


Fig.12(c)

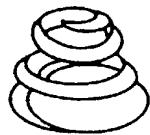


Fig.13

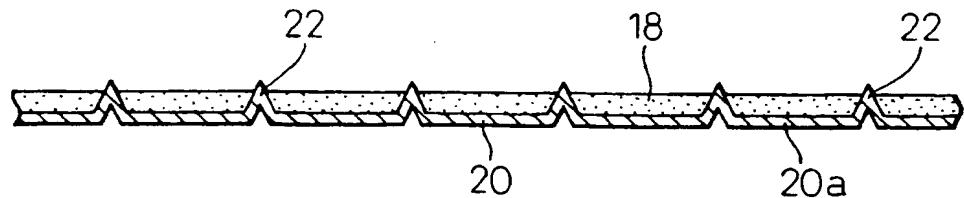


Fig.14

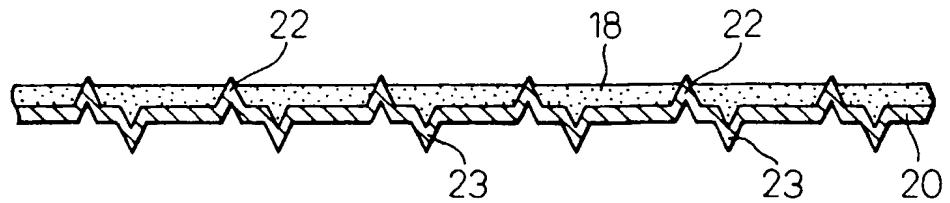


Fig.15

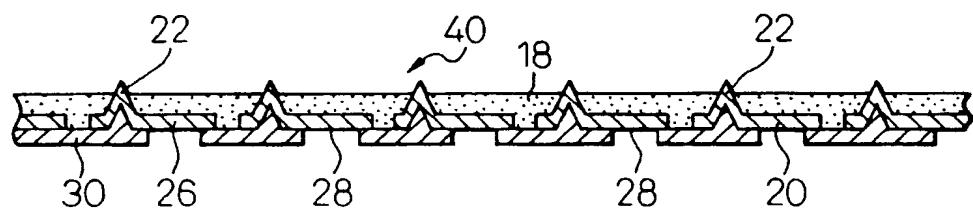


Fig.16

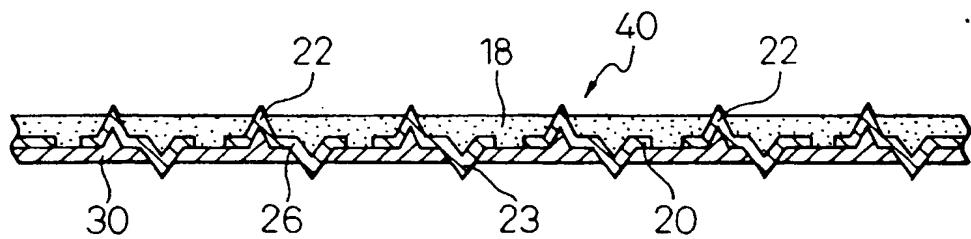


Fig.17

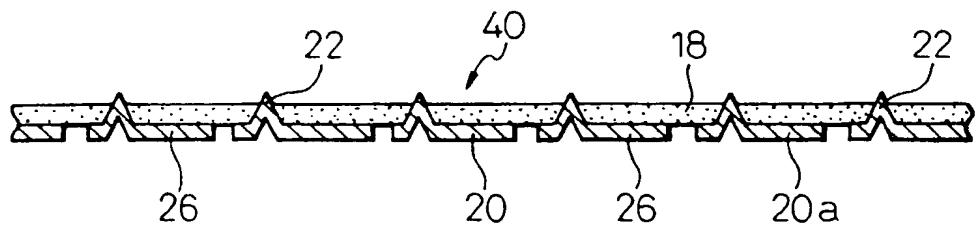


Fig.18

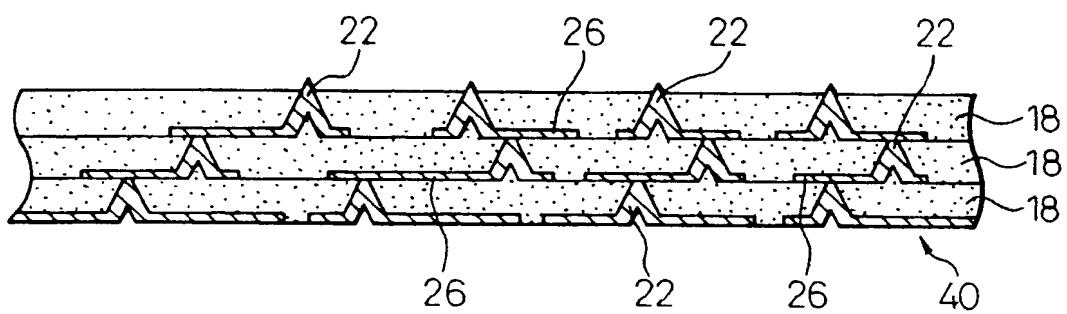


Fig.19(a1)

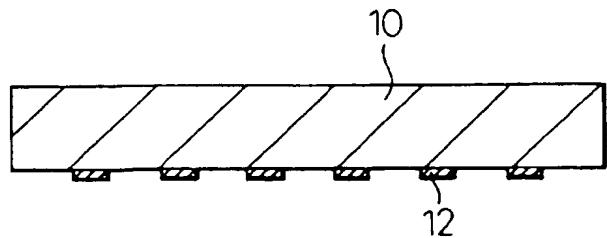


Fig.19(a2)

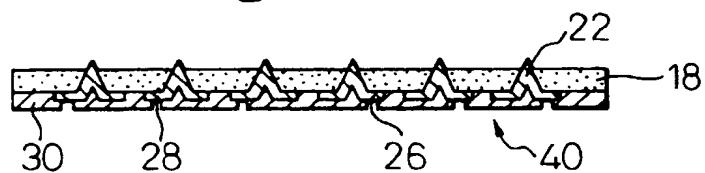


Fig.19(b)

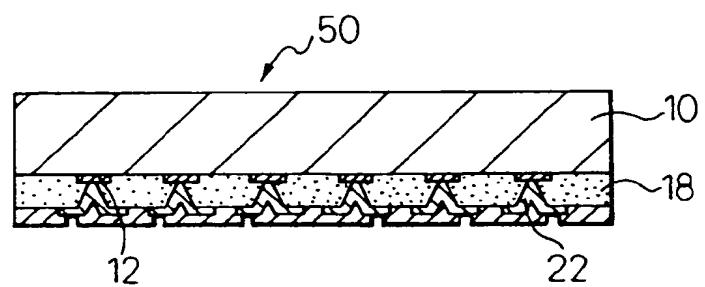


Fig.19(c)

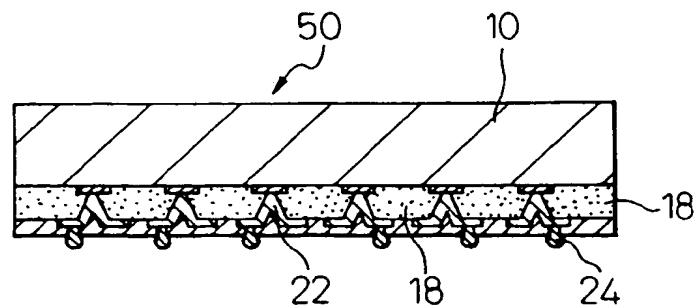


Fig.20

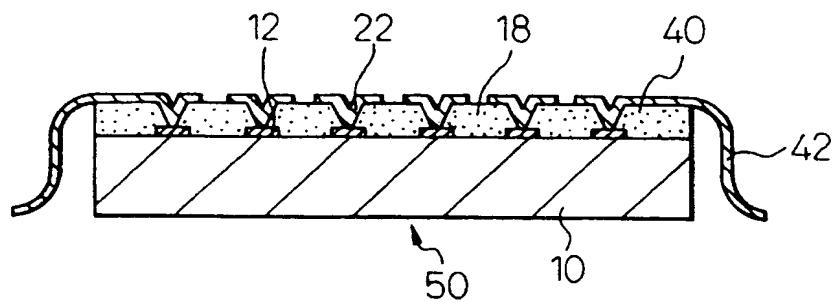


Fig.21

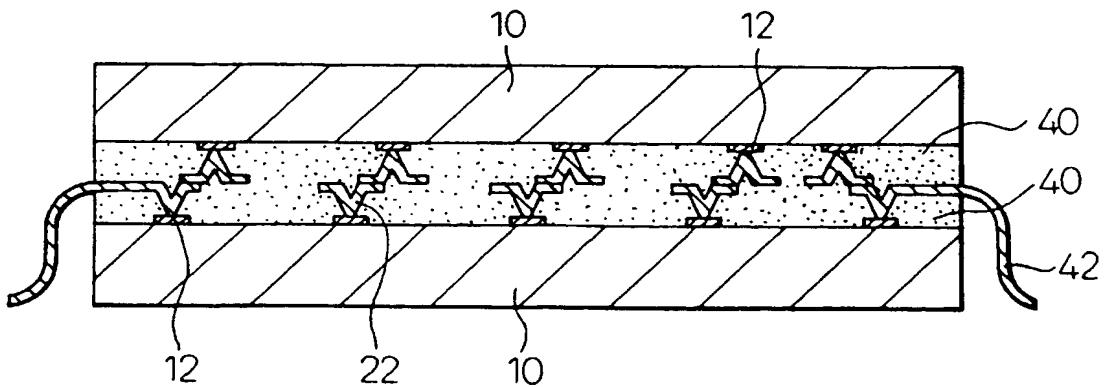
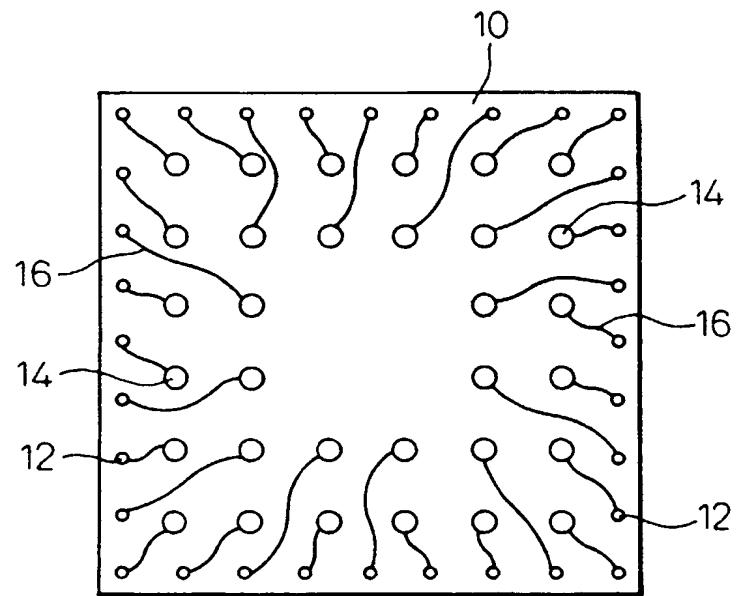


Fig.22

PRIOR ART



**THIS PAGE BLANK (USPTO)**



(19) Europäisches Patentamt  
European Patent Office  
Office européen des brevets



(11)

EP 1 005 086 A3

(12)

## EUROPEAN PATENT APPLICATION

(88) Date of publication A3:  
03.01.2001 Bulletin 2001/01

(51) Int Cl. 7: H01L 23/495, H01L 23/498

(43) Date of publication A2:  
31.05.2000 Bulletin 2000/22

(21) Application number: 99309372.3

(22) Date of filing: 24.11.1999

(84) Designated Contracting States:  
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU  
MC NL PT SE

Designated Extension States:  
AL LT LV MK RO SI

(30) Priority: 26.11.1998 JP 33509898

(71) Applicant: SHINKO ELECTRIC INDUSTRIES CO.  
LTD.  
Nagano-shi, Nagano 380-0921 (JP)

(72) Inventors:

- Muramatsu, Shigetsugu,  
Shinko Elect. Ind. Co. Ltd.  
Nagano-shi, Nagano 380-0921 (JP)
- Ogawa, Yoshihiko, Shinko Elect. Ind. Co. Ltd.  
Nagano-shi, Nagano 380-0921 (JP)
- Kojima, Norio  
Yokohama-shi, Kanagawa 235-0045 (JP)

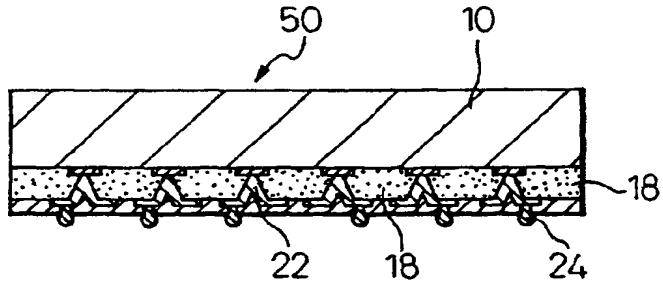
(74) Representative: Rackham, Stephen Neil  
GILL JENNINGS & EVERY,  
Broadgate House,  
7 Eldon Street  
London EC2M 7LH (GB)

### (54) Metal foil having bumps, circuit substrate having the metal foil, and semiconductor device having the circuit substrate

(57) A semiconductor device wherein a circuit substrate of a single or multiple layer is composed in such a manner that bumps (22), which are electrically connected to connection electrodes (12) provided on one face of a surface mount device (10), are arranged in the same planar arrangement as that of the connection electrodes (12). The bumps (22) protrude from one side

of a sheet of metal foil (20) on which wiring patterns (16) electrically connected to the bumps (22) are formed. An insulating adhesive agent layer (18) is adhered to the side of the sheet of metal foil (20) having the bumps (22) and is also adhered to one face of the surface mount device (10) while the tips of the bumps (22) come into contact with respective connection electrodes (12).

Fig.19(c)





European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number  
EP 99 30 9372

| DOCUMENTS CONSIDERED TO BE RELEVANT  |   |   |  |
|--|---|---|--|
| Category   | Citation of document with indication, where appropriate, of relevant passages   | Relevant to claim   | CLASSIFICATION OF THE APPLICATION (Int.Cl.7) |
| X  | US 5 148 265 A (KHANDROS IGOR Y ET AL)<br>15 September 1992 (1992-09-15)  | 1-5,<br>7-10, 12,<br>16-20  | H01L23/495<br>H01L23/498                     |
| Y  | * column 10, line 25-62 *   | 11,<br>13-15,<br>21-23  |  |
|  | * column 15, line 24 - column 17, line 55;<br>figure 9 *  |   |  |
| X  | US 5 706 174 A (KARAVAKIS KONSTANTINE ET AL)<br>6 January 1998 (1998-01-06)<br>* column 3, line 49 - column 5, line 51;<br>figures 1A,B * | 1-7, 10   |  |
| Y  | EP 0 649 171 A (HUGHES AIRCRAFT CO)<br>19 April 1995 (1995-04-19)<br>* column 10, line 4 - column 11, line 32;<br>figure 16 *             | 13-15,<br>21-23   |  |
| Y  | US 5 518 964 A (SMITH JOHN W ET AL)<br>21 May 1996 (1996-05-21)<br>* column 14, line 47 - column 15, line 43;<br>figure 17 *              | 11  | TECHNICAL FIELDS<br>SEARCHED (Int.Cl.7)      |
| A  | EP 0 529 577 A (HUGHES AIRCRAFT CO)<br>3 March 1993 (1993-03-03)<br>* figures 2-5 *   | 1-23  | H01L   |
| P, X   | US 5 896 271 A (SCHREIBER CHRIS M ET AL)<br>20 April 1999 (1999-04-20)<br>* figure 5 *  | 1, 13, 21   |  |
| <p>The present search report has been drawn up for all claims</p>  |   |   |  |
| Place of search  | Date of completion of the search  | Examiner  |  |
| MUNICH   | 9 November 2000   | Edmeades, M   |  |
| CATEGORY OF CITED DOCUMENTS  |   | T : theory or principle underlying the invention<br>E : earlier patent document, but published on, or<br>after the filing date<br>D : document cited in the application<br>L : document cited for other reasons<br>.....<br>& : member of the same patent family, corresponding<br>document |  |
| X : particularly relevant if taken alone<br>Y : particularly relevant if combined with another<br>document of the same category<br>A : technological background<br>O : non-written disclosure<br>P : intermediate document |   |   |  |

**ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.**

EP 99 30 9372

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.  
 The members are as contained in the European Patent Office EDP file on  
 The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

09-11-2000

| Patent document<br>cited in search report |   | Publication<br>date |  | Patent family<br>member(s)  | Publication<br>date  |
|---|---|---------------------|--|---|--|
| US 5148265                                | A | 15-09-1992          |  | US 5148266 A<br>AU 8731291 A<br>CA 2091438 A<br>EP 0551382 A<br>JP 2924923 B<br>JP 6504408 T<br>KR 9705709 B<br>US 5258330 A<br>US 5679977 A<br>WO 9205582 A<br>US 5852326 A<br>US 5685885 A<br>US 5347159 A<br>US 5848467 A<br>US 5950304 A<br>US 6133627 A<br>US 5682061 A<br>US 5346861 A  | 15-09-1992<br>15-04-1992<br>25-03-1992<br>21-07-1993<br>26-07-1999<br>19-05-1994<br>19-04-1997<br>02-11-1993<br>21-10-1997<br>02-04-1992<br>22-12-1998<br>11-11-1997<br>13-09-1994<br>15-12-1998<br>14-09-1999<br>17-10-2000<br>28-10-1997<br>13-09-1994   |
| US 5706174                                | A | 06-01-1998          |  | US 5801441 A<br>US 5518964 A<br>US 6012224 A<br>AU 3592895 A<br>EP 0800754 A<br>JP 10506236 T<br>WO 9609746 A<br>US 5659952 A<br>US 6133639 A<br>US 5915170 A<br>US 5959354 A<br>US 6104087 A<br>US 6117694 A<br>US 6080603 A<br>US 5688716 A<br>US 5830782 A<br>US 5913109 A<br>US 5989936 A<br>AU 2913595 A<br>EP 0870325 A<br>JP 2898265 B<br>JP 10256314 A<br>JP 3022949 B<br>JP 8055881 A<br>KR 211611 B<br>WO 9602068 A | 01-09-1998<br>21-05-1996<br>11-01-2000<br>09-04-1996<br>15-10-1997<br>16-06-1998<br>28-03-1996<br>26-08-1997<br>17-10-2000<br>22-06-1999<br>28-09-1999<br>15-08-2000<br>12-09-2000<br>27-06-2000<br>18-11-1997<br>03-11-1998<br>15-06-1999<br>23-11-1999<br>09-02-1996<br>14-10-1998<br>31-05-1999<br>25-09-1998<br>21-03-2000<br>27-02-1996<br>02-08-1999<br>25-01-1996 |

**ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.**

EP 99 30 9372

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on. The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

09-11-2000

| Patent document cited in search report |   | Publication date | Patent family member(s)  | Publication date   |
|--|---|------------------|--|--|
| EP 0649171                             | A | 19-04-1995       | US 5412539 A<br>JP 3069010 B<br>JP 7201902 A   | 02-05-1995<br>24-07-2000<br>04-08-1995   |
| US 5518964                             | A | 21-05-1996       | AU 2913595 A<br>EP 0870325 A<br>JP 2898265 B<br>JP 10256314 A<br>JP 3022949 B<br>JP 8055881 A<br>KR 211611 B<br>US 5959354 A<br>WO 9602068 A<br>US 6104087 A<br>US 6117694 A<br>US 6080603 A<br>US 5801441 A<br>US 5688716 A<br>US 5830782 A<br>US 5913109 A<br>US 5706174 A<br>US 6012224 A<br>US 5989936 A | 09-02-1996<br>14-10-1998<br>31-05-1999<br>25-09-1998<br>21-03-2000<br>27-02-1996<br>02-08-1999<br>28-09-1999<br>25-01-1996<br>15-08-2000<br>12-09-2000<br>27-06-2000<br>01-09-1998<br>18-11-1997<br>03-11-1998<br>15-06-1999<br>06-01-1998<br>11-01-2000<br>23-11-1999 |
| EP 0529577                             | A | 03-03-1993       | US 5207887 A<br>DE 69207996 D<br>DE 69207996 T<br>DE 69214389 D<br>DE 69214389 T<br>EP 0529578 A<br>JP 2072901 C<br>JP 5211218 A<br>JP 7105420 B<br>US 5354205 A<br>US 5307561 A<br>JP 2763715 B<br>JP 5198926 A   | 04-05-1993<br>14-03-1996<br>19-09-1996<br>14-11-1996<br>30-04-1997<br>03-03-1993<br>25-07-1996<br>20-08-1993<br>13-11-1995<br>11-10-1994<br>03-05-1994<br>11-06-1998<br>06-08-1993   |
| US 5896271                             | A | 20-04-1999       | NONE   |  |

**This Page is Inserted by IFW Indexing and Scanning  
Operations and is not part of the Official Record**

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- BLACK BORDERS**
- IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- FADED TEXT OR DRAWING**
- BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- SKEWED/SLANTED IMAGES**
- COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- GRAY SCALE DOCUMENTS**
- LINES OR MARKS ON ORIGINAL DOCUMENT**
- REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- OTHER:** \_\_\_\_\_

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.**

**THIS PAGE BLANK (USPTO)**